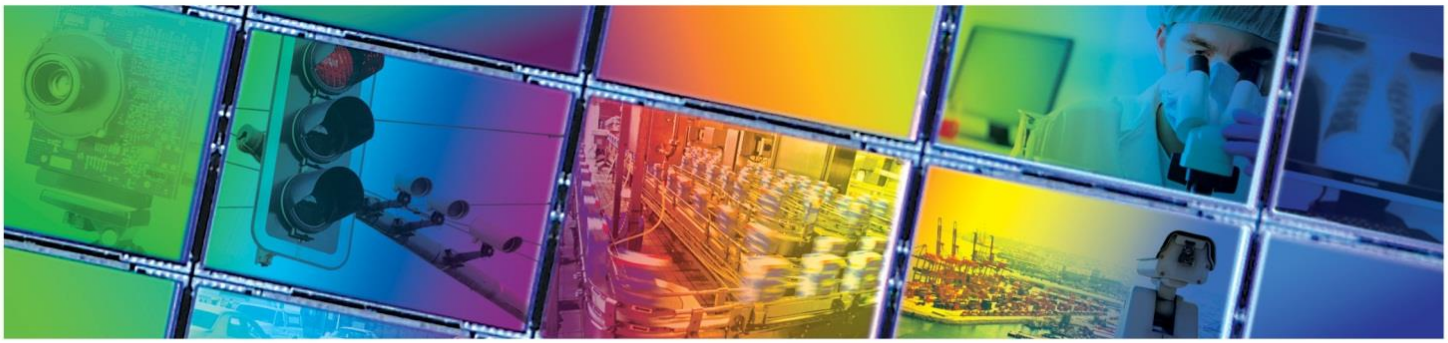
ON Semiconductor®

KLI-2113 IMAGE SENSOR

LINEAR CCD IMAGE SENSOR



JUNE 12, 2014

DEVICE PERFORMANCE SPECIFICATION

REVISION 3.1 PS-0050

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Summary Specification

KLI-2113 Image Sensor

DESCRIPTION

The KLI-2113 Image Sensor is a high dynamic range, multispectral, linear CCD image sensor ideally suited for demanding color scanner applications.

The imager consists of three parallel 2098-element photodiode arrays—one for each primary color. The KLI-2113 sensor offers high sensitivity, a high data rate, low noise, and negligible lag. Independent exposure control for each channel allows color balancing at the front end. CMOS-compatible 5 V clocks, and single 12 V DC supply are all that are required to drive the KLI-2113 sensor, simplifying the design of interface electronics.

FEATURES

- High Resolution
- Wide Dynamic Range
- High Sensitivity
- High Operating Speed
- High Charge Transfer Efficiency
- No Image Lag
- Electronic Exposure Control
- Pixel Summing Capability
- Up to 2.0V peak-peak Output
- 5.0V Clock Inputs
- Two-Phase Register Clocking
- On-chip Dark Reference

APPLICATIONS

- Digitization
- Machine Vision
- Mapping/Aerial
- Photography

Parameter	Typical Value
Architecture	3 Channel, RGB Tri-linear CCD
Pixels Count	2098 x 3
Pixel Size	14 µm (H) x 14 µm (V)
Pixel Pitch	14 µm
Inter-Array Spacing	112 mm (8 lines effective)
Imager Size	29.37 mm (H) x 0.24 mm (V)
Saturation Signal	170,000 electrons
Dynamic Range	76 dB
Responsivity (Wavelength = 460, 540, 650 nm)	25, 32, 50 V/µJ/cm^2
Output Sensitivity	11.5 µV/electron
Dark Current	0.02 pA/pixel
Dark Current Doubling Rate	9 °C
Charge Transfer Efficiency	0.99999/Transfer
Photoresponse Non-uniformity	5% Peak-Peak
Lag (First Field)	0.6%
Maximum Data Rate	20 MHz/Channel
Package	CERDIP (Sidebrazed, CuW)
Cover Glass	AR coated, 2 sides

Parameters above are specified at T = 25°C and 2 MHz clock rates unless otherwise noted.

Ordering Information

Catalog Number	Product Name	Description	Marking Code
4H0602	KLI- 2113-AAA-ER-AA	Monochrome, No Microlens, CERDIP Package (leadframe), Taped Clear Cover Glass with AR coating (2 sides), Standard Grade	KLI-2113-AAA (Serial Number)
4H0605	KLI- 2113-AAA-ER-AE	Monochrome, No Microlens, CERDIP Package (leadframe), Taped Clear Cover Glass with AR coating (2 sides), Engineering Sample	
4H0601	KLI- 2113-AAB-ED-AA	Monochrome, No Microlens, CERDIP Package (leadframe), Clear Cover Glass with AR coating (both sides), Standard Grade	KLI-2113-AAB (Serial Number)
4H0604	KLI- 2113-AAB-ED-AE	Monochrome, No Microlens, CERDIP Package (leadframe), Clear Cover Glass with AR coating (both sides), Engineering Sample	
4H0600	KLI- 2113-DAA-ED-AA	Color (RGB), No Microlens, CERDIP Package (leadframe), Clear Cover Glass with AR coating (both sides), Standard Grade	KLI-2113-DAA (Serial Number)
4H0603	KLI- 2113-DAA-ED-AE	Color (RGB), No Microlens, CERDIP Package (leadframe), Clear Cover Glass with AR coating (both sides), Engineering Sample	
4H0096	KEK-4H0096-KLI-2113-12-5	Evaluation Board (Complete Kit)	N/A

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

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Phone: (585) 784-5500
E-mail: info@truesenseimaging.com

Device Description

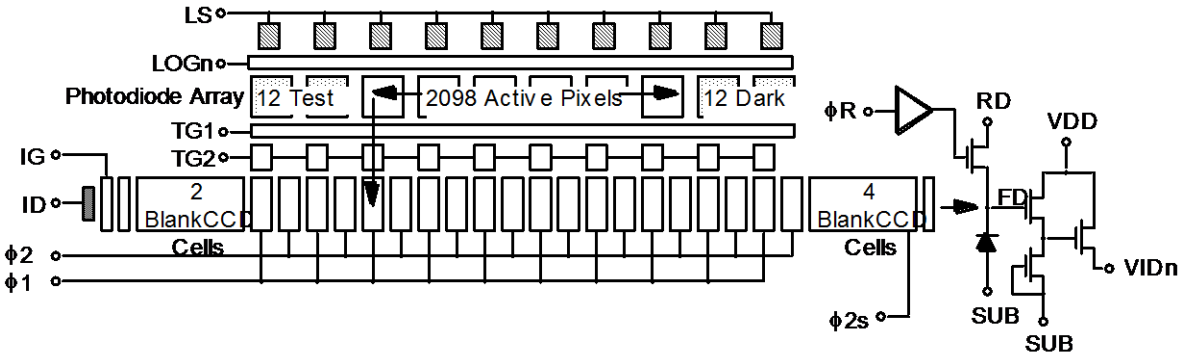


Figure 1: Single Channel Schematic

Exposure Control

Exposure control is implemented by selectively clocking the LOG gates during portions of the scanning line time. By applying a large enough positive bias to the LOG gate, the channel potential is increased to a level beyond the 'pinning level' of the photodiode. (The 'pinning' level is the maximum channel potential that the photodiode can achieve and is fixed by the doping levels of the structure.) With TG1 in an 'off' state and LOG strongly biased, all of the photocurrent will be drawn off to the LS drain. Referring to Figure 6, one notes that the exposure can be controlled by pulsing the LOG gate to a 'high' level while TG1 is turning 'off' and then returning the LOG gate to a 'low' bias level sometime during the line scan. The effective exposure (t_{exp}) is the net time between the falling edge of the LOG gate and the falling edge of the TG1 gate (end of the line). Separate LOG connections for each channel are provided, enabling on-chip light source and image spectral color balancing. As a cautionary note, the switching transients of the LOG gates during line readout may inject an artifact at the sensor output. Rising edge artifacts can be avoided by switching LOG during the photodiode-to-CCD transfer period, preferably, during the TG1 falling edge. Depending on clocking speeds, the falling edge of the LOG should be synchronous with the φ1/φ2 shift register readout clocks. For very fast applications, the falling edge of the LOG gate may be limited by on-chip RC delays across the array. In this case, artifacts may extend across one or more pixels. Correlated double sampling (CDS) processing of the output waveform can remove the first order magnitude of such artifacts. In high dynamic range applications, it may be advisable to limit the LOG fall times to minimize the current transients in the device substrate and limit the magnitude of the artifact to an acceptable level.

Pixel Summing

The effective resolution of this sensor can be varied by enabling the pixel summing feature. A separate pin is provided for the last shift register gate labeled φ2s. This gate, when clocked appropriately, stores the summation of signal from adjacent pixels. This combined charge packet is then transferred onto the sense node. As an example, the sensor can be operated in 2-pixel summing mode (1049 pixels), by supplying a φ2s clock which is a 75% duty cycle signal at 1/2 the frequency of the φ2 signal, and modifying the φR clock as depicted in Figure 8. Applications that require full resolution mode (2098 pixels), must tie the φ2s pin to the φ2 pin. Refer to Figure 7and Figure 8 for additional details.

IMAGE ACQUISITION

During the integration period, an image is obtained by gathering electrons generated by photons incident upon the photodiodes. The charge collected in the photodiode array is a linear function of the local exposure. The charge is stored in the photodiode itself and is isolated from the CCD shift registers during the integration period by the transfer gates TG1 and TG2, which are held at barrier potentials. At the end of the integration period, the CCD register clocking is stopped with the φ1 and φ2 gates being held in a 'high' and 'low' state respectively. Next, the TG gates are turned 'on' causing the charge to drain from the photo-diode into the TG1 storage region. As TG1 is turned back 'off', charge is transferred through TG2 and into the φ1 storage region. The TG2 gate is then turned 'off', isolating the shift registers from the accumulation region once again. Complementary clocking of the φ1 and φ2 phases now resumes for readout of the current line of data while the next line of data is integrated.

CHARGE TRANSPORT

Readout of the signal charge is accomplished by two-phase, complementary clocking of the Phase 1 and Phase 2 gates (φ1 and φ2) in the horizontal (output) shift register. The register architecture has been designed for high speed clocking with minimal transport and output signal degradation, while still maintaining low ($4.75V_{p-p}$min) clock swings for reduced power dissipation, lower clock noise and simpler driver design. The data in all registers is clocked simultaneously toward the output structures. The signal is then transferred to the output structures in a parallel format at the falling edge of the φ2s clock. Resettable floating diffusions are used for the charge to voltage conversion while source followers provide buffering to external connections. The potential change on the floating diffusion is dependent on the amount of signal charge and is given by $\Delta VFD = \Delta Q/C_{FD}$, where ΔVFD is the change in potential on the floating diffusion, ΔQ is the amount of charge, and C_{FD} is the capacitance of the floating diffusion node. Prior to each pixel output, the floating diffusion is returned to the RD level by the reset clock, φR.

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

Pin	Name	Description
1	VIDR	Red Output Video
2	SUB	Substrate
3	RD	Reset Drain
4	φR	Reset Clock
5	LOGR	Red Overflow Gate
6	LOGG	Green Overflow Gate
7	SUB	Substrate
8	N/C	No Connection
9	LS	Light Shield/Exposure Drain
10	IG	Input Gate/LOG Test Pin
11	TG2	Outer Transfer Gate
12	N/C	No Connection
13	φ2s	Phase2 Shift Register Summing Gate Clock
14	φ2	Phase2 Shift Register Clock

Pin	Name	Description
28	VIDG	Green Output Video
27	SUB	Substrate
26	VDD	Amplifier Supply
25	VIDB	Blue Output Video
24	SUB	Substrate
23	N/C	No Connection
22	LOGB	Blue Overflow Gate
21	N/C	No Connection
20	N/C	No Connection
19	ID	Input Diode Test Pin
18	TG1	Inner Transfer Gate
17	N/C	No Connection
16	N/C	No Connection
15	φ1	Phase1 Shift Register Clock

Imaging Performance

Typical Operational Conditions

Specifications given under nominal operating conditions @ 25 °C ambient, f_{CLK} =2 MHz and nominal external VIDn load resistors unless otherwise specified.

Specifications

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Verification Plan
Saturation Output Voltage	V_{sat}		2.0		V_{p-p}	1, 7	die[8]
Output Sensitivity	$\Delta V_o/\Delta N_e$		11.5		$\mu V/e^-$	7	design[9]
Saturation Signal Charge	$N_{e,sat}$		170k		electrons		design[9]
Responsivity (@ 650nm) (@ 540nm) (@ 460nm)	R		50 32 25		$V/\mu J/cm^2$	2, 7	design[9]
Output Buffer Bandwidth	f_{-3dB}		75		MHz	@ C_{LOAD} = 10 pF	design[9]
Dynamic Range	DR		76		dB	3	design[9]
Dark Current	I_{dark}		0.02		pA/pixel	4	die[8]
Charge Transfer Efficiency	CTE		.99999		-	5	design[9]
Lag	L		0.6	1	%	1st Field	design[9]
DC Output Offset	V_{odc}	6	7	9	Volts	7	design[9]
Photoresponse Uniformity	PRNU		5	10	% p-p	6	die[8]
Register Clock Capacitance	C_φ		500		pF	per phase	design[9]
Transfer Gate Capacitance	C_{TG}		400		pF		design[9]

Notes:

1. Defined as the maximum output level achievable before linearity or PRNU performance is degraded.
2. With color filter. Values specified at filter peaks. 50% bandwidth = ±30 nm.
3. This device utilizes 2-phase clocking for cancellation of driver displacement currents. Symmetry between φ1 and φ2 phases must be maintained to minimize clock noise.
4. Dark current doubles approximately every +9 °C.
5. Measured per transfer. For total line h < $(.99999)^{4256}$ =0.96
6. Low frequency response across array with color filter array.
7. Decreasing external VIDn load resistors to improve signal bandwidth will decrease these parameters.
8. A parameter that is measured on every sensor during production testing.
9. A parameter that is quantified during the design verification activity.

Typical Performance Curves

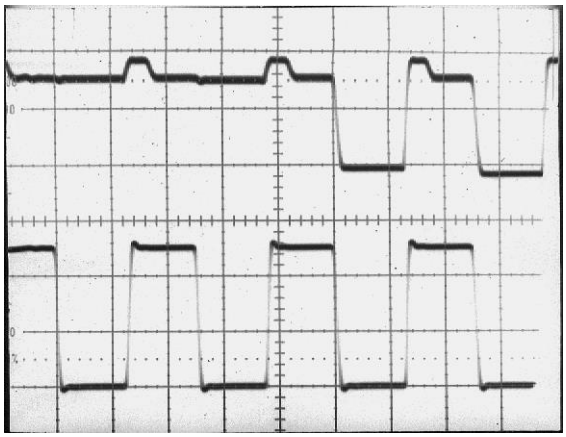
(2 MHz Operation, Emitter Follower Buffered, 3/4 Vsat, Dark to Bright Transition)

VIDR Output

(1V/DIV)

φ2 Clock

(2V/DIV)



Time (200 ns/DIV)

Figure 2: Output Waveforms

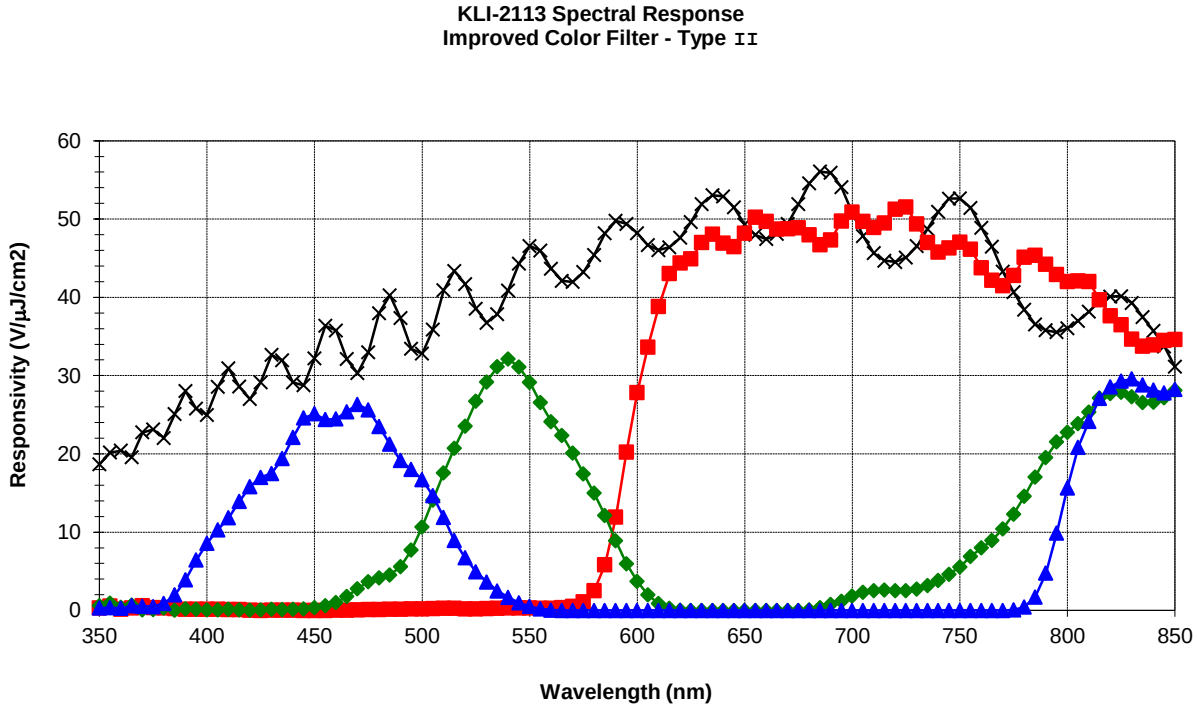


Figure 3: Typical Responsivity

Defect Definitions

Operationing Conditions

Test conditions: T=25 °C, f_{CLK}=2MHz, t_{int}=1.066msec.

Specifications

Field	Defect Type	Threshold	Units	Notes	Number
Dark	Bright	8.0	mV	1, 2	0
Bright	Bright/Dark	10	%	1, 3	0
Bright	Exposure Control	4.0	mV	1, 4, 5	≤16

Notes:

1. Defective pixels will be separated by at least one non-defective pixel within and across channels.
2. Pixels whose response is greater than the average response by the specified threshold. See Figure 4 below.
3. Pixels whose response is greater or less than the average response by the specified threshold. SeeFigure 4below.
4. Pixels whose response deviates from the average pixel response by the specified threshold when operating in exposure control mode. See Figure 4 below.
5. Defect coordinates are available upon request.

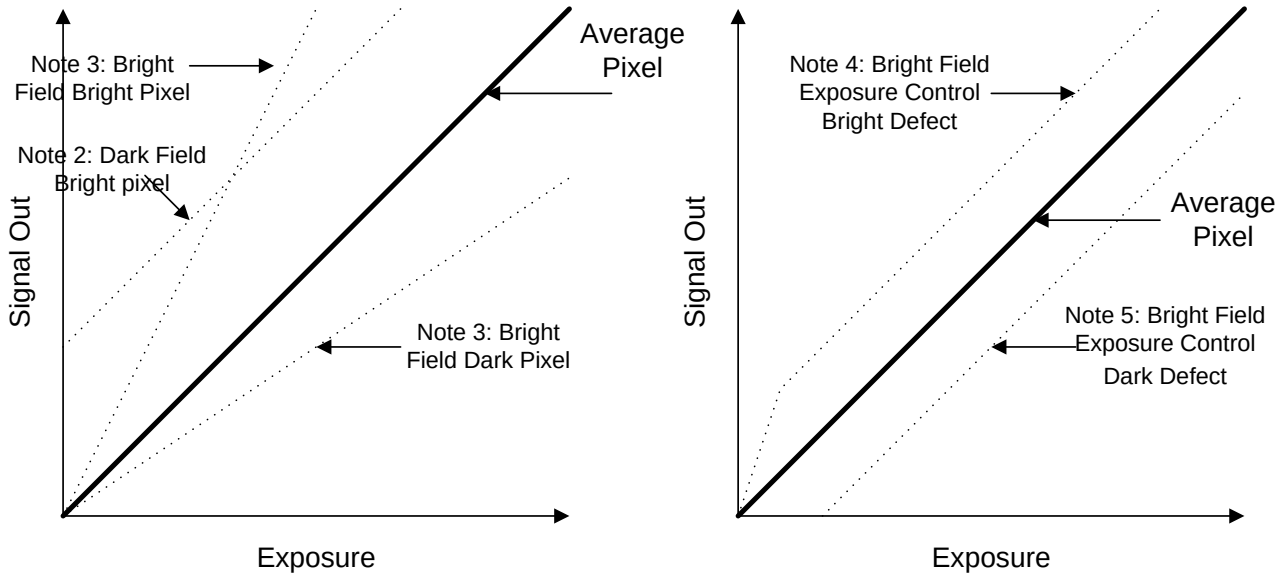


Figure 4: Illustration of Defect Classifications

Operation

ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Gate Pin Voltages	V_{GATE}	-0.5	+16	V	1, 2
Pin to Pin Voltage	$V_{PIN-PIN}$		16	V	1, 3
Diode Pin Voltages	V_{DIODE}	-0.5	+16	V	1,4
Output Bias Current	I_{DD}		-10	mA	5
Output Load Capacitance	$C_{VID,LOAD}$		15	pF	
CCD Clocking Frequency	f_C		20	MHz	6

Notes:
1. Referenced to substrate voltage.
2. Includes pins: φ1, φ2, φ2s, TG1, TG2, φR, IG, and LOGn.
3. Voltage difference (either polarity) between any two pins.
4. Includes pins: VIDn, RD, VDD, LS and ID.
5. Care must be taken not to short output pins to ground during operation as this may cause serious damage to the output structures.
6. Charge transfer efficiency will degrade at frequencies higher than the nominal (2MHz) clocking frequency. VIDn load resistor values may need to be decreased as well to achieve required output bandwidths.

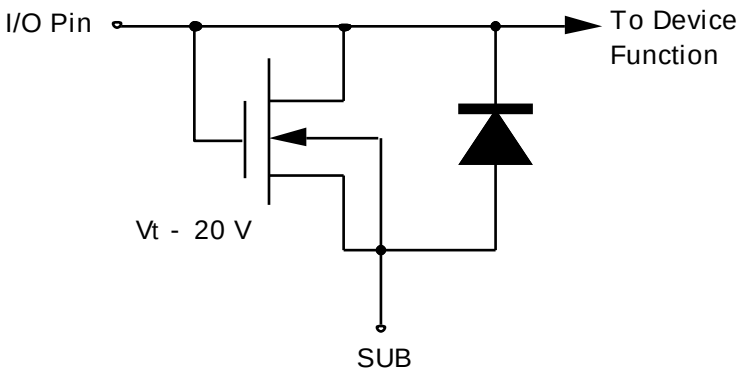


Figure 5: ESD Protection Circuit

CAUTION:

To allow for maximum performance, this device contains limited i/o protection and may be sensitive to electrostatic induced damage. Devices should be installed in accordance with strict ESD handling procedures!

DC Bias Operating Conditions

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Substrate	VSUB		0		V	
Reset Drain Bias	VRD	+11.5	+12.0	+12.5	V	
Output Buffer Supply	VDD	+11.5	+12.0	+12.5	V	
Light Shield/Drain Bias	VLS	+11.5	+12.0	+12.5	V	
Output Bias Current/Ch.	IDDn	-4.0	-6.0	-8.0	mA	1
Test Pin-Input Gate/LOG	VIG		+12.0		V	
Test Pin-Input Diode	VID		+12.0		V	

Notes:

1. A current sink must be supplied for each output. Load capacitance should be minimized so as not to limit bandwidth.See Figure 6.Choose values optimized for specific operating frequency, but R2 should not be less than 75Ω.

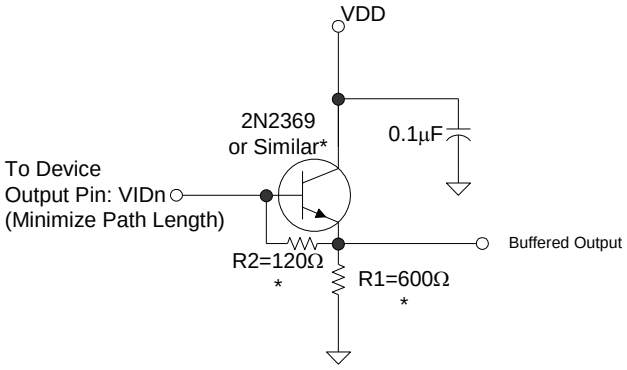


Figure 6: Typical Output Bias/Buffer Circuit

AC Operating Conditions

Clock Levels

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
CCD Readout Clocks High	$V_{\phi 1H}$, $V_{\phi 2H}$, $V_{\phi 2sH}$	+4.75	+5.0	+5.25	V	
CCD Readout Clocks Low	$V_{\phi 1L}$, $V_{\phi 2L}$, $V_{\phi 2sL}$	-0.1	0	+0.1	V	
Transfer Clocks High	V_{TG1H}, V_{TG2H}	+4.75	+5.0	+5.25	V	
Transfer Clocks Low	V_{TG1L}, V_{TG2L}	-0.1	0	+0.1	V	
Reset Clock High	$V_{\phi RH}$	+4.75	+5.0	+5.25	V	
Reset Clock Low	$V_{\phi RL}$	-0.1	0	+0.1	V	
Exposure Clocks High	V_{LOG1H}, V_{LOG2H}	+4.75	+5.0	+5.25	V	1
Exposure Clocks Low	V_{LOG1L}, V_{LOG2L}	-0.1	0	+0.1	V	1

Notes:
1. Tie pin to 0 V for applications where exposure control is not used.

AC Timing Levels

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
CCD Element Duration	$1e^-(= 1/f_{CLK})$	50	500		ns	
Line/Integration Period	$1L (= t_{int})$	0.108	1.066		ms	
PD-CCD Transfer Period	t_{pd}	1.0			µs	
Transfer Gate 1 Clear	t_{tg1}	500			ns	
Transfer Gate 2 Clear	t_{tg2}	500			ns	
LOGGate Duration	t_{LOG1}	1			µs	
LOGGate Clear	t_{LOG2}	1			µs	
Reset Pulse Duration	t_{rst}	9			ns	
Clamp to φ2 Delay	t_{cd}	5			ns	1
Sample to Reset Edge Delay	t_{sd}	5			ns	1
CCD Clock Rise Time	t_r		30		ns	Typical

Notes:
1. Recommended delays for correlated double sampling of output.

Timing

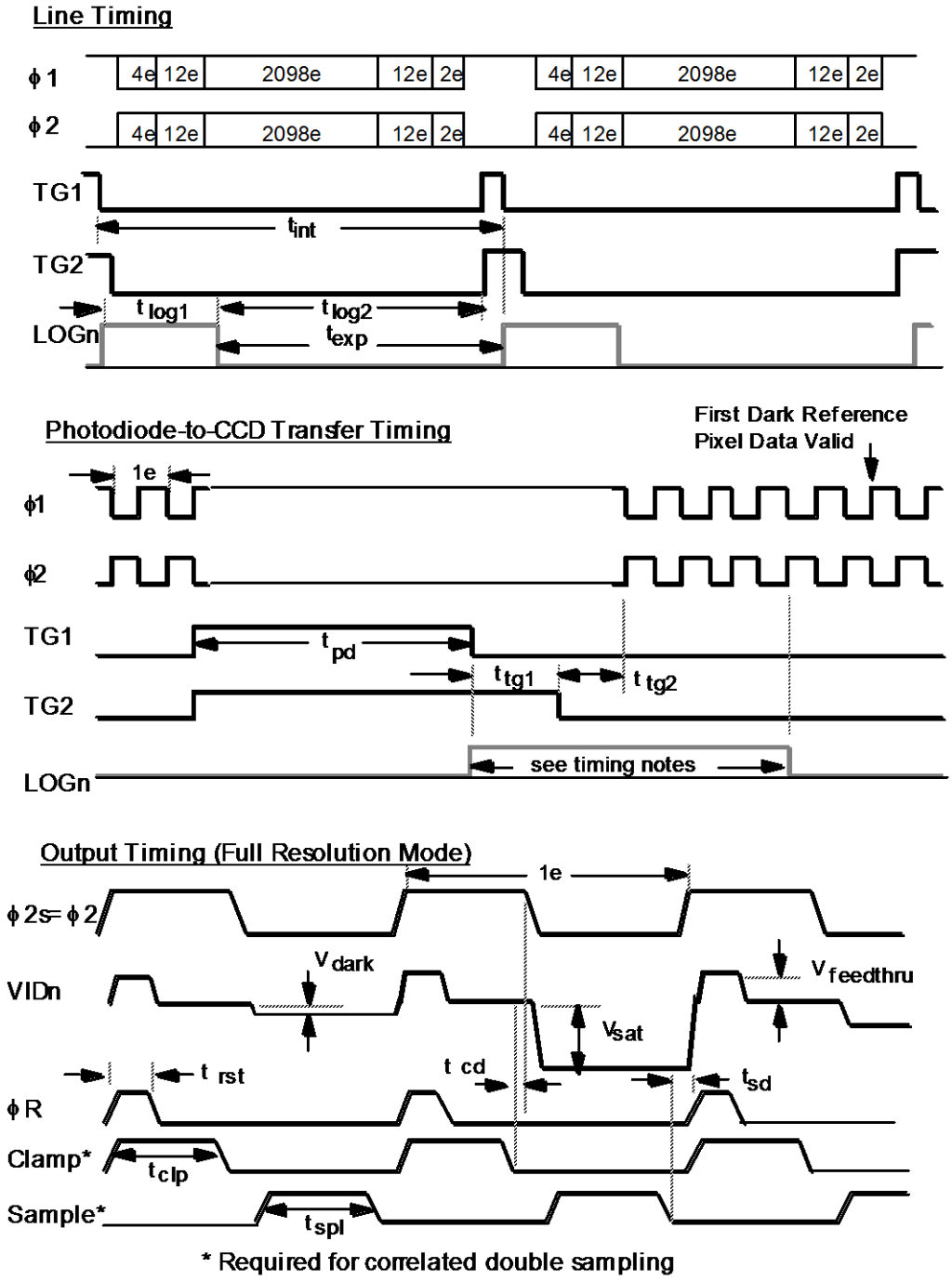


Figure 7: Normal ModeTiming

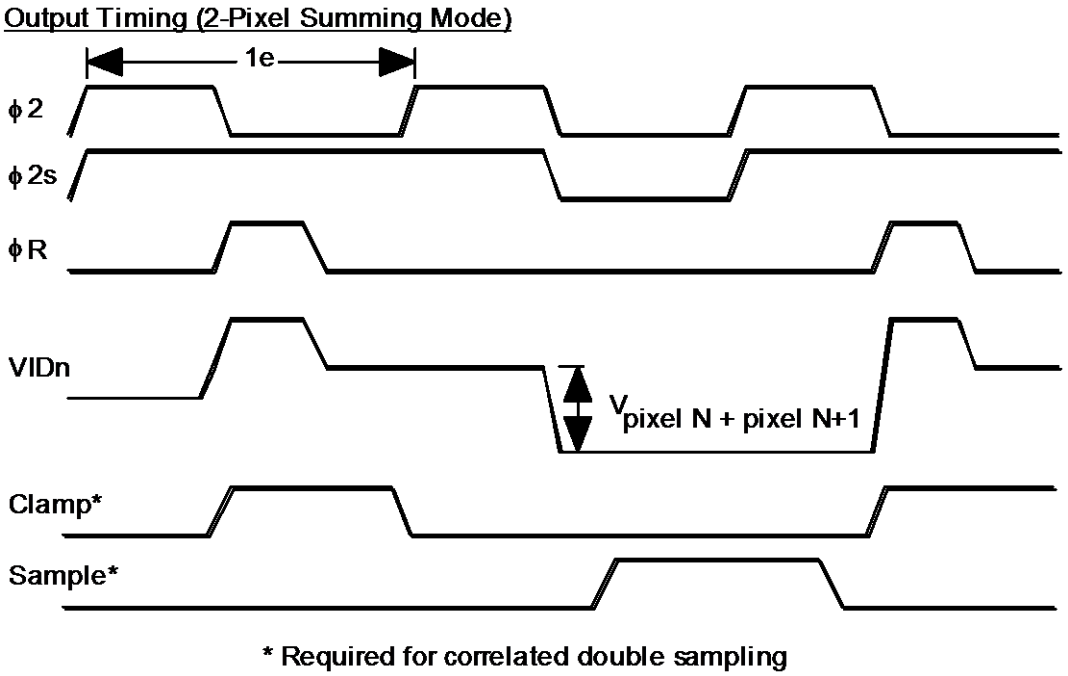


Figure 8: Binning ModeTiming

Storage and Handling

Storage Conditions

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	0	70	°C	1
Operating Temperature	T_{OP}	-25	+80	°C	2

Notes:
1. Noise performance will degrade with increasing temperatures.
2. Long term storage at these temperatures will accelerate color filter degradation.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

Cover Glass Care and Cleanliness

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

Environmental Exposure

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

Soldering Recommendations

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30W soldering iron. Heat each pin for less than 2 seconds duration.

Mechanical Information

COMPLETED ASSEMBLY

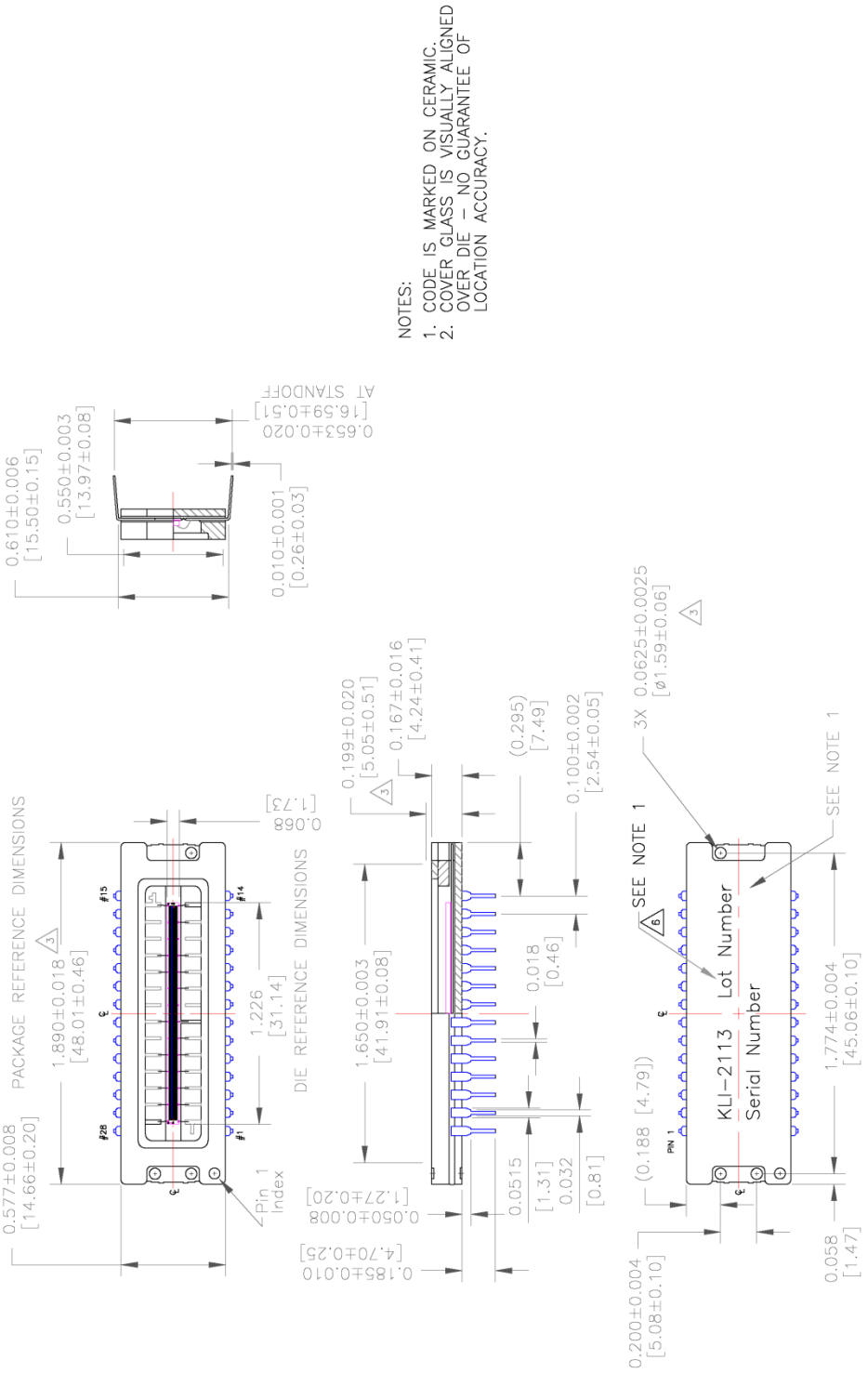


Figure 9: Completed Assembly Drawing (1 of 4)

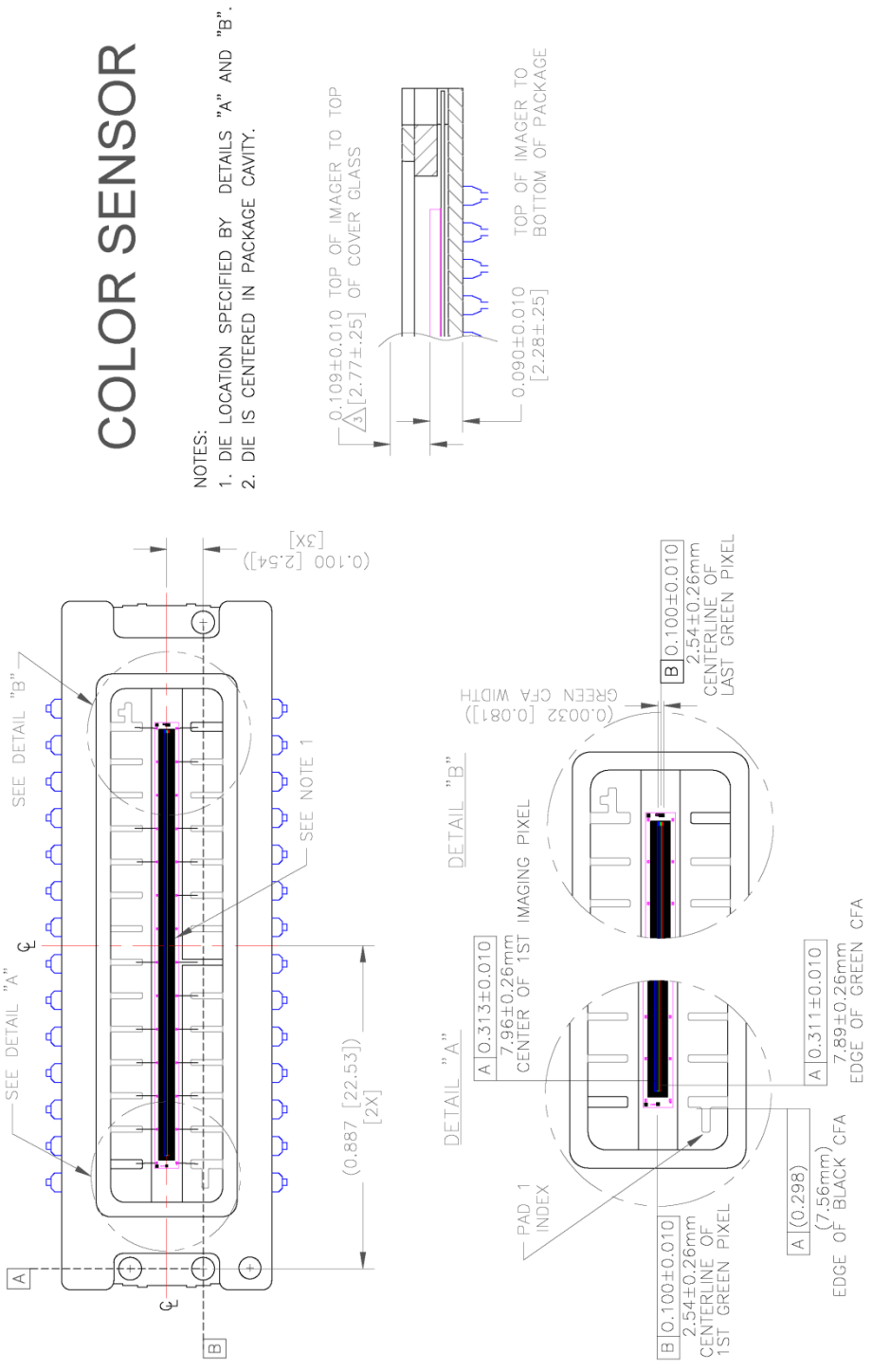


Figure 10: Completed Assembly Drawing (2 of 4)

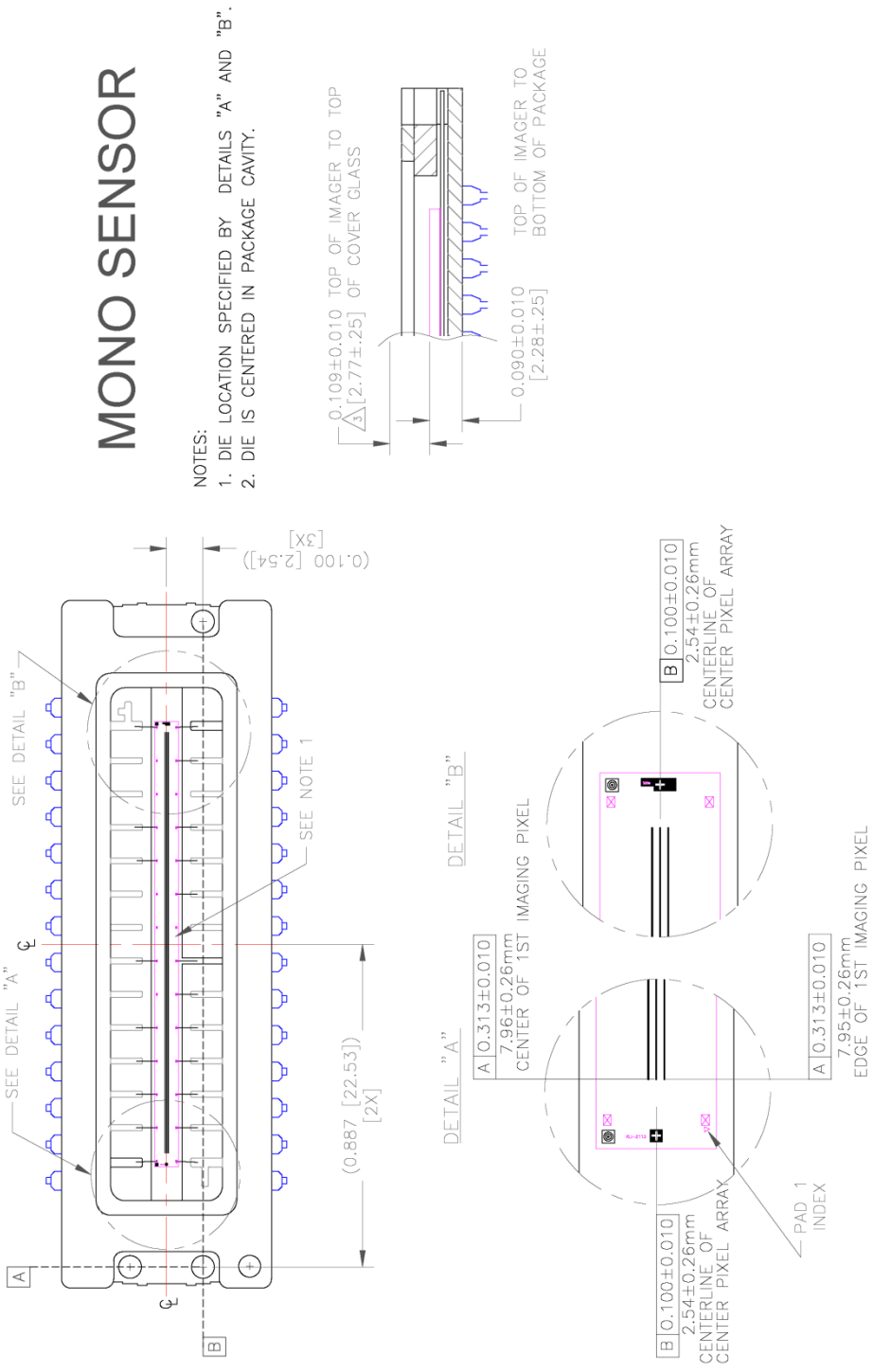


Figure 11: Completed Assembly Drawing (3 of 4)

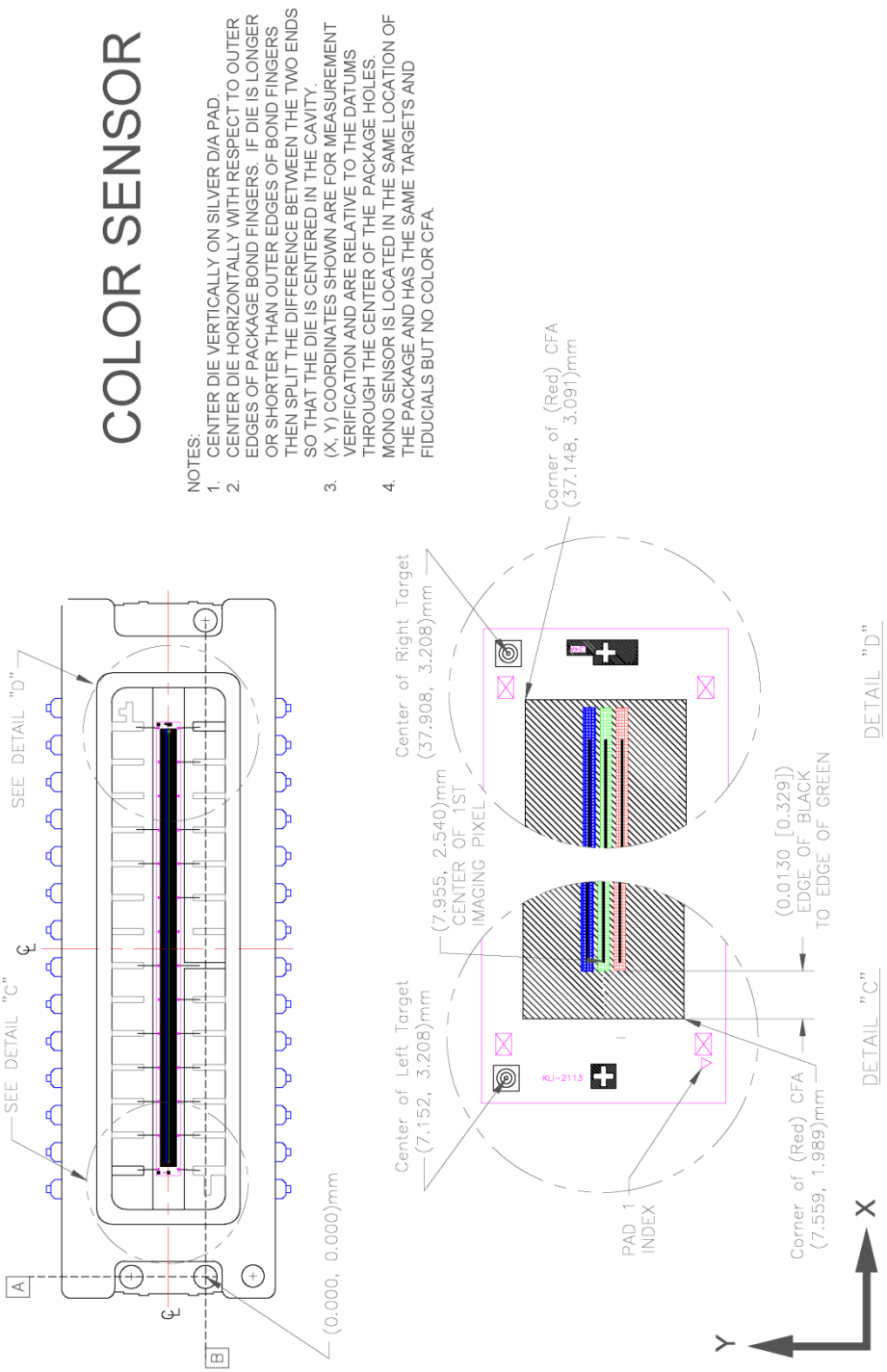


Figure 12: Completed Assembly Drawing (4 of 4)

Quality Assurance and Reliability

Quality and Reliability

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

Replacement

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

Liability of the Supplier

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

Liability of the Customer

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Test Data Retention

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.

Revision Changes

MTD/PS-0229

Revision Number	Description of Changes
4	• New Color Filter materials implemented.
5	• Updated format. Added Serial Numbers to Package Drawings
5.1	• Corrected responsivity in Table on p.4

PS-0050

Revision Number	Description of Changes
1.0	• Initial release with new document number, updated branding and document template • Updated *Storage and Handling* and *Quality Assurance and Reliability* sections
2.0	• Updated assembly drawing
3.0	• Updated assembly drawing
3.1	• Updated branding

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

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